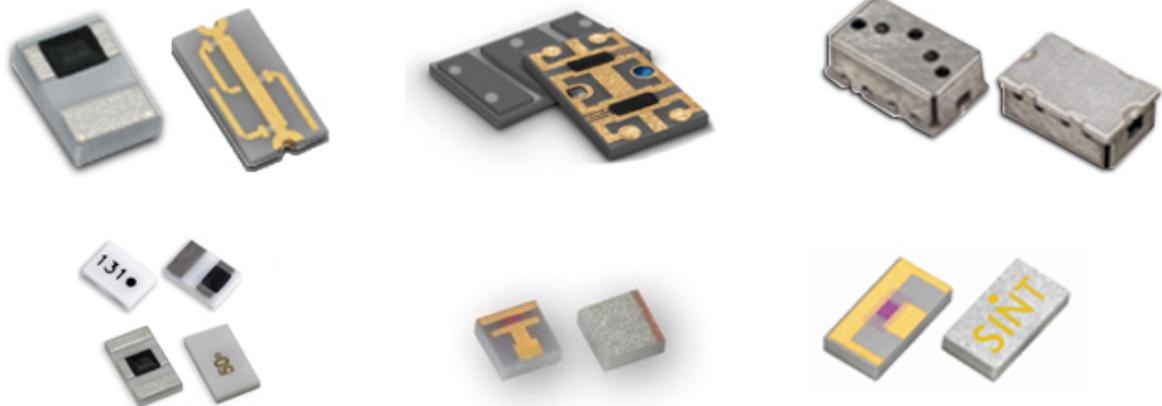


# White Paper

SMT Board Level Components

## Fixture Preparation and RF Test of SMT Board Level Components at High Frequencies

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## 1. Contents

2.	Abstract .....	3
3.	Introduction .....	3
4.	Simulation .....	4
5.	Test Fixture Choice .....	6
6.	Mounting Consideration.....	7-7
7.	Test Considerations .....	9-9
8.	Conclusion.....	10-10

## 2. Abstract

*Abstract — As the applications in modern telecommunications shift beyond 20 GHz, so does the need for RF components and systems at these frequencies. To properly support introduction of new technologies at frequencies of K-band, Ku-band and further towards millimeter wave, all aspects of component design and development must be considered including high frequency fixturing and probing and production testing. With the operational frequency increase, sizes of surface mount chip components shrink while DUT-to-test board air gaps become more critical. This and similar dimensional constraints create significant issue for a production test technician and therefore require serious consideration and analysis. This paper presents some of the results of such an analysis performed on RF passive components installed in either surface mount configuration and with or without the wire bond interface. Various surface mount interfaces, number of wires in wire bond interface, and DUT positional tolerances were analyzed and their impact on the RF performance and thermal management considered. In addition to destructive tests, a few non-destructive (push-on) fixtures were discussed and proposed. Finally, recommendations are given as to how to properly mount these miniature-size RF passive components to maximize their performance in a real-world application.*

*Index Terms — RF resistive, SMT interface, wire bond, epoxy, solder, thermal management.*

## 3. Introduction

The telecommunications industry and community have been dealing with the issue of radio spectrum allocation and congestion for many years. Radio spectrum represents a natural resource whose allocation must be carefully managed to achieve its optimal use. It is well known that with the introduction of various new applications over radio frequencies, the radio spectrum became congested over the last few decades. For example, it turns out that more than two thirds of all Wi-Fi devices use 2.4 GHz band completely ignoring 5.8 GHz band that is allocated for the same application. The issue of spectrum congestion is amplified in geographical areas where population is high or where there are many application users [1]. The engineering community has been proposing various techniques to tackle the issue of better spectrum efficiency [2] and higher data rates [3].

The most natural way to reduce the problem is by allocating higher frequencies to the new applications. This shift of the radio wave ecosystem towards higher frequencies of millimetre wave comes at a heavy price; RF devices are getting increasingly smaller and challenging to be produced and tested. The dimensional resolution increases linearly with the frequency increase. For example, a 5-mil airgap at 40 GHz produces the same

electrical effect as a 50-mil airgap at 4 GHz. The challenges briefly described above must be addressed throughout the entire design and development cycle – from simulation to production to test. New design techniques must be applied through RF simulation tools, more controlled manufacturing processes developed, and more accurate test fixtures and test procedures utilized.

## 4. Simulation

To properly analyze the impact of the test fixture on the electrical performance of a device under test (DUT), a chip RF termination has been selected with an operational frequency band DC-30 GHz. The termination is realized on an Aluminium Nitride (AlN) substrate of with a 10-mil thickness (Fig 1a). This is a standard surface mount (SMT) component that is mounted by using a soldering process for a good thermal management. The interface to the application (test) board is established through a wire or ribbon bond process with an optimum of three wires or ribbon of the same width installed on the input pad of the termination. The electrical performance of the RF termination is optimized to provide a voltage standing wave ratio of 1.20:1 over a broad band DC – 30 GHz (Fig 1b).

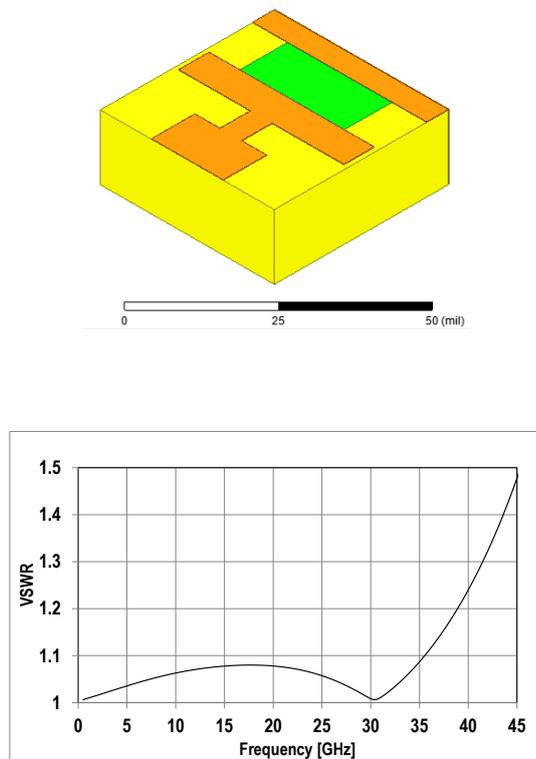


Fig. 1. Surface mount RF termination: (a) model in Ansys HFSS, (b) simulated nominal RF performance (VSWR).

Once nominal design has been tuned, various scenarios have been analyzed to evaluate the impact of the interface between the termination and the application board (Fig. 2).

Both the ribbon bond and wire bond have been taken into consideration. The cases that were of special interest in this tolerance analysis were the ribbon bond width and height, the number and size of the wire bonds, the thickness of the application board, and the air gap between the termination and the application board. As expected at these frequencies, the interface plays a crucial role in the performance of the termination and if not tuned properly, it may introduce a significant undesired reflection (Fig. 3).

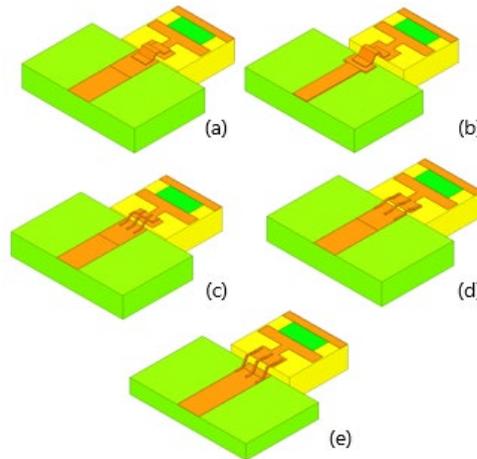


Fig. 2. Various tolerance scenarios: (a) ribbon bond (b) ribbon bond and air gap, (c) three wire bonds with significant height, (d) low height wire bonds, (e) thin application board.

The simulation show that the optimal performance would occur for no gap between the application board and the termination while ribbon (or wire bond) must spread over the entire width of the trace underneath. The application board must be positioned so that its top surface plane is at the same level as the top surface plane of the termination.

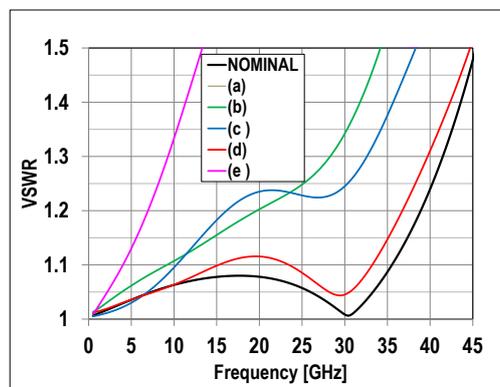


Fig. 3. Simulated electrical performance for the scenarios shown in Fig 2 (a) – (e)

## 5. Test Fixture Choice

In order to properly fixture the presented RF termination and similar high frequency surface mount components for RF performance verification testing, the information about the medium (substrate) onto which the device will be mounted on during its intended field operation is needed. This is achieved by spending effort in first constructing a 'good' 50  $\Omega$  transmission through line with the line width sized to match the width of the DUT. The properties of PCB substrate such as dielectric constant and thickness are chosen to yield a transmission line that closely matches the DUT I/O pad widths. To reduce radiation losses, most of the test boards are realized in a grounded coplanar waveguide (CPWG) structure that exhibits better performance than the traditional microstrip line test fixtures at frequencies above 20 GHz. In addition to the argument above, CPWG lines also work very well with SMT (surface-mount) devices since the signal and ground are located on the same plane. The through line test fixture should be sized to match the final DUT test fixture size. Essentially, the through line length will be the size of the input launch times two.

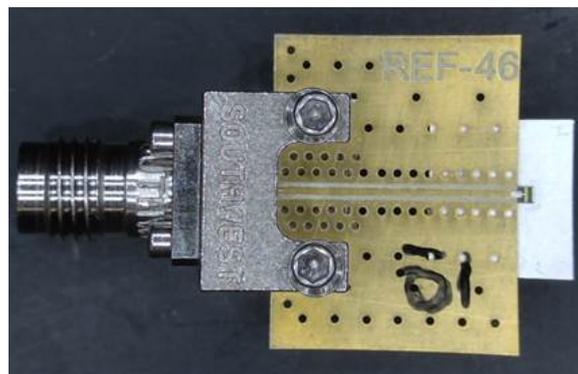


Fig. 4. The test fixture used to test the presented RF termination

The DUT test fixture length will be the through line length plus the DUT length for 2-port devices. A single port device, such as a termination fixture length will be that one launch length (half of the through line) plus the DUT length. The substrate thickness should be selected properly for the frequency of interest to avoid the creation of higher order modes that appear as undesired spikes on the display of the vector network analyzer (VNA).

The through line fixture will also include some sort of coaxial connector and a transition from planar board into the coaxial structure of the connector (Fig 4). The connector is chosen to support the operation frequency band and desired VSWR. It consists of a transition plate that holds the pin centered on the round dielectric to form a coaxial structure. The planar-to-coaxial transition must be carefully optimized to reduce

undesired reflections. This is obtained through an iterative process consisting of a multiple simulation and test steps. The test is performed through analysis of reflections in a time domain on a Vector network Analyzer (VNA) with TDR (Time Domain Reflectometry) capabilities. We have found that PCB edge-mount connectors with built-in transition plates have proven to be more consistent than connectors with separate piece parts that are assembled in the test lab. These “single-piece” fully assembled connectors have been already optimized for a given performance by the connector supplier. On the other side, the connectors assembled by the test operators in the test lab often suffer unacceptable performance fluctuations due to the increased possibility for variation through component and assembly tolerances.

## 6. Mounting Consideration

First step in properly mounting the DUT for testing is to carefully inspect all the components of the test fixture to be assembled. Special attention should be given to the test board edges (Fig 5a). Common PCB manufacturing often leave rough edges that can cause fixture assembly issues. The edges of the test board can usually be cleaned up using fine grit sandpaper. (Fig 5b).

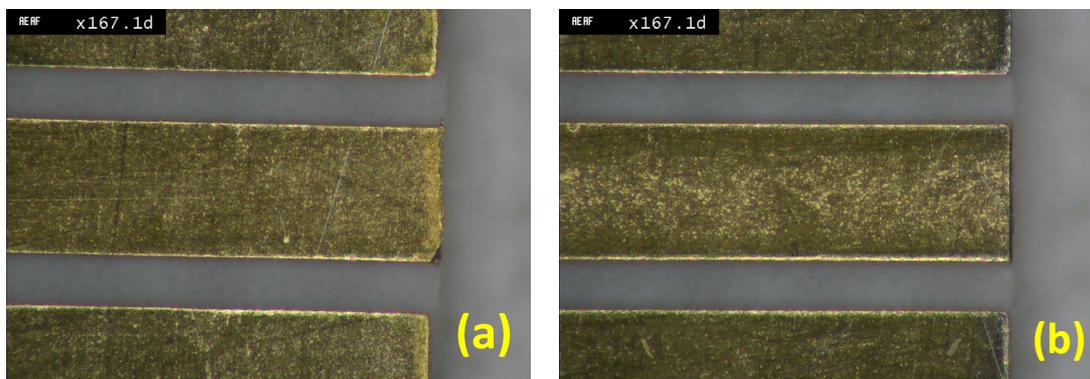


Fig. 5. Test board transmission line: (a) rough edge (before cleaning), (b) smooth edge (after cleaning)

Next is the fixture assembly; the carrier board is soldered to the test board using Sn96 solder. Care should be taken to insure there is no solder run-out into the area where the DUT is to be mounted. The final step in the fixture assembly is to mount the connector to the test board. Things to look for at this step is to center the connector pin on the transmission line and to ensure the connector is flush with the edge of the test board to avoid undesired air gaps (Fig 6). Use of a microscope is essential to ensuring that the connector is mounted properly.

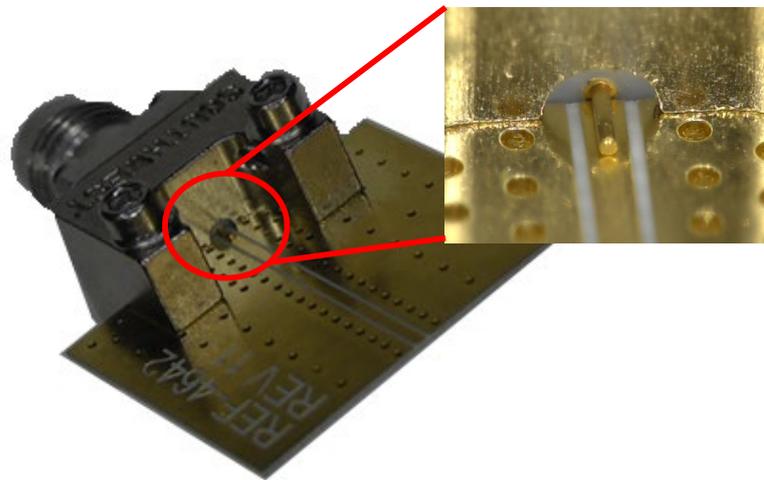


Fig. 6. Connector pin alignment on the test board

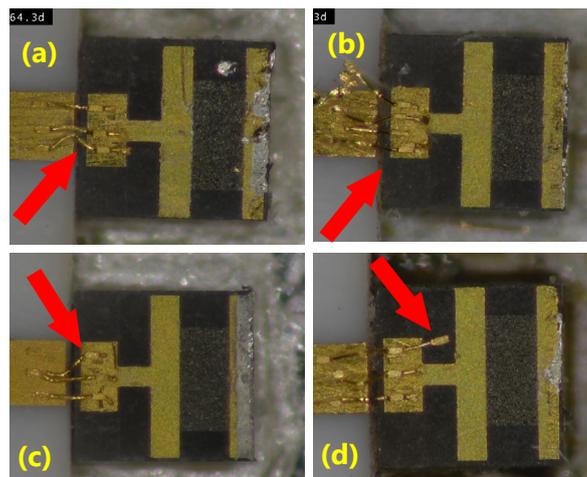


Fig. 7. Bad mounting practices: (a) poor wire bond connection to the pad, (b) air gap between the termination and the application board, (c) poor wire bond, (d) wire bond sticking out of the pad area

Having a properly assembled test fixture it is time to mount the DUT. The DUT should also be inspected to ensure the edges are cleanly cut and have no jagged edges prior to being installed on the test fixture. Due to possible power handling requirements the DUT needs to be soldered in place. This presents challenges in proper alignment to the transmission line. When soldering, the DUT tends to move during solder reflow. To prevent this, pure indium solder could be used. The indium solder is very soft and the DUT can be pressed into the solder before reflow which allows for fine adjustment of the DUT to the transmission line and insure the DUT is flush with the test board. When the DUT is reflowed, it remains in place. Finally, the DUT need to be connected to the transmission line. There are primarily two types of connection methods, ribbon and wire

bonding. Short ribbon bonds provide the best RF performance, but wire bonding is the most popular. In order to analyze the effects of the different connection methods it is important to use the same DUT. This can prove difficult as removing the ribbon or wire bonds can often damage the circuit. In order to prevent any damage, the ribbon bond can be replaced with a small piece of indium solder. The indium solder does not need to be reflowed just pressed into place. The pliability of the indium allows for good contact to the transmission line and DUT. It can then be easily removed and replaced with the wire bonds. This allows for a direct comparison of the effects of the different connection methods using the identical DUT and fixture. All good assembly practice start playing an extremely important role at high frequencies. As the simulation analysis showed, a small tolerances or changes in the shape and position of wire bonds, for example, can result in significant deterioration of electrical performance at high frequencies. Bad wire bond and other mounting practices (Fig 7) result in significant reflections that “mask” the true performance of the DUT. On the other side, proper installation (Fig 8) results in a good correlation between the designer’s simulation and the tested prototype.

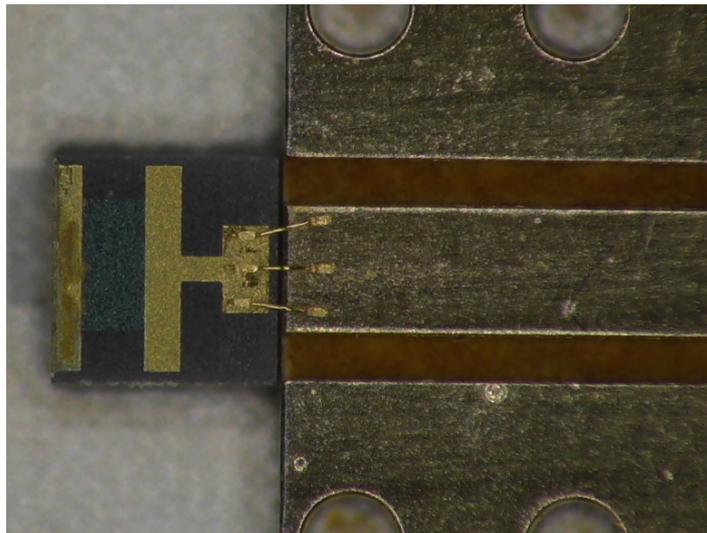


Fig. 8. Properly installed RF termination on the test fixture; good correlation between the simulated model and the prototype

## 7. Test Considerations

It is always best to measure any component with a test fixture whose performance exceeds the DUT. This may not always be the case, especially at all frequencies in a broadband sweep, since the fixture’s physical length will natively resonate and cause significant reflections at some frequencies. These undesired effects can be removed using strategically placed RF absorber material. This solution is a last resort as it most of time turns out to be costly, cumbersome and of varied effectiveness. Another method

used to remove unwanted fixture effects from measurement is using the gating function of TDR enabled equipment. The gating function is often used to disregard the reflections caused by the test fixture.

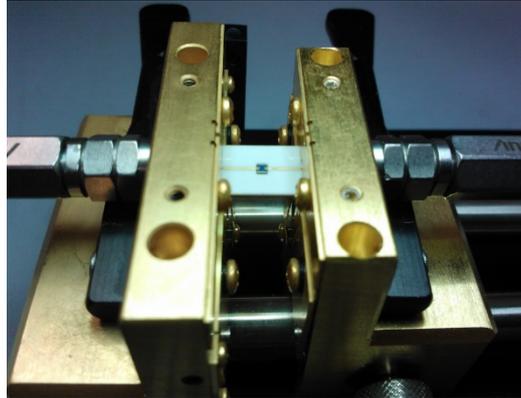


Fig. 9 Anritsu Universal Test Fixture (UTF) used in many high frequency test applications

In production RF test, DUTs must be verified for RF performance by test methods that use non-solder contact of signal and ground pads. This test method is referred to as 'push-on' testing. The development of a push-on test fixture in addition to the design of an RF component is an essential part of each project. This approach results in an establishment of a good correlation between soldered and non-soldered performance of the tested RF component as the PCB is the same structure in both measurements. Having a push-on fixture enables a non-destructive test that is required in many applications. The non-destructive test fixture may be fully developed and tailored to a specific design or a standardized pre-manufactured test fixture used (Fig 9).

## 8. Conclusion

In order to meet challenges of the spectrum congestion and higher data rates in the telecommunications of the 21st century, RF engineering is shifting its focus towards the development of RF components that operate at increasingly higher frequencies. To be successful with this endeavor, new simulation techniques and test methodologies are required; those that take into account specific behavior of electromagnetic waves at frequencies of K-band and above. This development must be a conjoint effort of all functional roles in the design and development of RF devices – engineering, manufacturing and test. Traditional separation in the development of the test fixture and a DUT does not exist anymore; the test fixture in a sense electrically becomes the part of the DUT that affects its performance. This poses a significant challenge as the electrical performance of an RF device can be guaranteed only in a specific environment. Collaboration between RF component development team and their customer is a

paramount in this process. Through this collaboration, all the necessary information about the application of the to-be-developed RF component must be discussed within the norms of intellectual property protection agreed between the two teams. Once established, this information is to be used to optimize the RF component for the best possible performance.

#### REFERENCES

- [1] S. Berger, "Spectrum Congestion – Is It a Technical Problem?", *2014 United States National Committee of URSI National Radio Science Meeting*, January 8-11, 2014.
- [2] R.L. Hinkle, "Spectrum conservation techniques for future telecommunications", *IEEE International Symposium on Electromagnetic Compatibility*, August 21-23, 1990.
- [3] R. De Keulenaer et al., "Measurements of millimeter wave test structures for high speed chip testing", *2014 IEEE 18<sup>th</sup> Workshop on Signal and Power Integrity (SPI)*, May 2014.
- [4] Rosas, B., "Optimizing Test Boards for 50 GHz End Launch Connectors: Grounded Coplanar Launches and Through Lines on 30-mil Rogers RO4350B with Comparison to Microstrip", Southwest Microwave Inc., Tempe, AZ, 2007. (Website: <https://mpd.southwestmicrowave.com/>)
- [5] Rosas, B., "Utilizing Time Domain (TDR) Test Methods for Maximizing Microwave Board Performance", Southwest Microwave Inc., Tempe, AZ, 2009. (Website: <https://mpd.southwestmicrowave.com/>)